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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/505,563	03/16/2005	Joerg Barthel	10191/3781	2444

26646 7590 12/04/2006

KENYON & KENYON LLP
ONE BROADWAY
NEW YORK, NY 10004

EXAMINER	
SPITTLE, MATTHEW D	

ART UNIT	PAPER NUMBER
2111	

DATE MAILED: 12/04/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/505,563	BARTHEL ET AL.	
	Examiner	Art Unit	
	Matthew D. Spittle	2111	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 March 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *16-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *16-30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *13 October 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *8/23/2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claims 16 – 30 have been examined.

Specification

The disclosure is objected to because of the following informalities: Page 7, line 32 recites "...physical unit." Examiner believes this should recite "...electronic unit."

Appropriate correction is required.

Claim Objections

Claim 30 is objected to because of the following informalities: Claim 30 contains a misspelling of the word "electronic" in line 3. Appropriate correction is required.

Claim Rejections - 35 USC § 101

35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

Claim 29 is rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter. Computer programs claimed as computer listings per se, i.e., the descriptions or expressions of the programs, are not physical "things." They are neither computer components nor statutory processes, as they are not "acts" being performed. Such claimed computer programs do not define any structural and functional interrelationships between the computer program and other claimed elements of a

computer, which permit the computer program's functionality to be realized. In contrast, a claimed computer-readable medium encoded with a computer program is a computer element which defines structural and functional interrelationships between the computer program and the rest of the computer which permit the computer program's functionality to be realized, and is thus statutory. See Lowry, 32 F.3d at 1583-84, 32 USPQ2d at 1035.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 23, 25, 27 and 28 are rejected under 35 U.S.C. 102(b) as being anticipated by Rossum et al.

Regarding claim 23, Rossum et al. describe a memory device, comprising:

A first memory area subdivided into pages (Figure 3, item 18);

A second memory area (interpreted as a page table; column 1, lines 53 – 55 and column 5, line 17 both describe a page table in the memory), the first memory area being intended for data (interpreted as wavetable data; column 2, lines 2 – 4), and physical addresses of the pages of the first memory area being stored in the second memory area (Examiner notes that the page table contains the mapping to the physical addresses, as evidenced by column 3, lines 10 – 13).

Regarding claim 25, Rossum et al. describe a motherboard of an electronic arithmetic-logic unit, comprising:

A processor (Figure 1, item 10);

A main memory (Figure 1, item 18) coupled to the processor via a bus (Figure 1, items 12, 16), the main memory including a first memory area divided into pages (Figure 3, item 18) and a second memory area storing physical addresses of the pages of the first memory area (interpreted as a page table; column 1, lines 53 – 55 and column 5, line 17 both describe a page table in the memory).

Regarding claim 27, Rossum et al. describe a system comprising:

An electronic unit (Figure 1, item 42);

A memory device (Figure 1, item 18) connected to the electronic unit via a data bus (Figure 1, items 22, 16), the memory device including:

A first memory area subdivided into pages (Figure 3, item 18);

A second memory area (interpreted as a page table; column 1, lines 53 – 55 and column 5, line 17 both describe a page table in the memory), the first memory area being intended for data (interpreted as wavetable data; column 2, lines 2 – 4), and physical addresses of the pages of the first memory area being stored in the second memory area (Examiner notes that the page table contains the mapping to the physical addresses, as evidenced by column 3, lines 10 – 13).

Regarding claim 28, Rossum et al. describe an electronic device, comprising:

An electronic arithmetic-logic unit (Figure 1, item 10);

A memory device (Figure 1, item 18), the memory device including a first memory area subdivided into pages (Figure 3, item 18) and a second memory area (column 1, lines 53 – 55 and column 5, line 17 both describe a page table in the memory), the first memory area being intended for data (interpreted as the wavetable data; column 2, lines 2 – 4), and physical addresses of the pages of the first memory area being stored in the second memory area (Examiner notes that the page table contains the mapping to the physical addresses, as evidenced by column 3, lines 10 – 13);

An electronic unit (Figure 1, item 42);

Wherein the electronic arithmetic-logic unit, the memory device, and the electronic unit are integrated in one component (Examiner identifies the one component being a "computer system." Column 2, line 23).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claims 16 – 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Rossum et al. (U.S. 5,864,876) in view of Porterfield (U.S. 6,301,645).

Regarding claim 16, Rossum et al. teach a method for transferring data via a data bus (Figures 1 and 2, item 22) between a memory device (Figure 1, item 18) and an electronic unit (Figure 1, item 42) via a data bus, the memory device including a first memory area subdivided into pages (Figure 3, item 18) and a second memory area (column 1, lines 53 – 55 and column 5, line 17 both describe a page table in the memory), the pages being accessed using physical address of the pages (column 2, lines 48 – 50), the first memory area being intended for storing data (interpreted as the wavetable data; column 2, lines 2 – 4) and the second memory area containing the physical addresses of the pages of the first memory area (Examiner notes that the page

table contains the mapping to the physical addresses, as evidenced by column 3, lines 10 – 13);

Transferring data between the memory device and the electronic unit (Examiner notes that reads and writes both require the transfer of data between the peripheral device and memory; column 2, lines 46 – 48);

Rossum et al. fail to teach during the data transfer, autonomously transferring the physical addresses from the second memory area to the electronic unit.

Porterfield teaches autonomously transferring physical addresses from the second memory area (interpreted as a remapping table; column 3, lines 23 – 32) to the electronic unit (interpreted as a source device and an address translator; Figure 4, item 405 describes transferring the physical addresses from the second memory area to the electronic unit during a data transfer. The motivation for this method, using the system controller of Porterfield, is to allow device requests to memory to be more efficient and maintain compatibility between different bus standards (column 1, lines 45 – 58). For this reason, Examiner finds that the device of Porterfield is applicable to the multi-device, multi-bus system of Rossum et al. (as shown in Figure 1).

Therefore, it would have been obvious to one of ordinary skill in this art at the time of invention by Applicant to incorporate the system controller of Porterfield into the system of Rossum et al. for the purpose of making data transfers between devices and memory more efficient, while maintaining compatibility between different devices and different bus standards. This would have been obvious to improve the performance of the system of Rossum et al.

Regarding claim 17, Porterfield teaches the additional limitation wherein at a beginning of the data transfer, a starting address of the second memory area is transmitted to the electronic unit (column 4, lines 30 – 41).

Regarding claim 18, Rossum et al. teach the additional limitation wherein during the data transfer, data from the electronic unit is written into the memory device (column 2, lines 46 – 50).

Regarding claim 19, Rossum et al. teach the additional limitation wherein during data transfer, data stored in the memory device is read by the electronic unit (column 2, lines 46 – 50).

Regarding claim 20, Rossum et al. teach the additional limitation wherein the data bus is a PCI bus (column 2, line 28).

Regarding claim 21, Rossum et al. teach the additional limitation wherein the memory device is a main memory (column 2, line 26; Figure 1, item 18), and a plug-in card is provided as the electronic unit (column 2, lines 38 – 39). Rossum et al. fail to explicitly teach a motherboard of an electronic arithmetic-logic unit, and an expansion slot. Examiner takes official notice that it is old and well known in this art for computer systems to include a CPU (Figure 1, item 10), memory (Figure 1, item 18), and multiple

busses (Figure 1, items 22, 40, 12, 16) on a motherboard that includes PCI expansion slots for peripheral devices (that may be implemented on a board; such as a soundboard or a graphics board; column 1, lines 30 – 32).

Regarding claim 22, Rossum et al. teach the additional limitation wherein the physical addresses are transferred to the electronic unit by DMA transfer (column 2, lines 48 – 50).

* * *

Claim 24 is rejected under 35 U.S.C. 103(a) as being unpatentable over Rossum et al. (U.S. 5,864,876) in view of what is old and well known in the art.

Regarding claim 24, Rossum et al. teach a method of using a memory device, comprising:

Providing a main memory (Figure 1, item 18), the main memory including a first memory area divided into pages (Figure 3, item 18);

Performing a data transfer using the main memory (column 2, lines 46 – 50).

Rossum et al. fail to explicitly teach a motherboard of an electronic arithmetic-logic unit. Examiner takes official notice that it is old and well known in this art for computer systems to include a CPU (Figure 1, item 10), memory (Figure 1, item 18), and multiple busses (Figure 1, items 22, 40, 12, 16) on a motherboard.

* * *

Claim 26 is rejected under 35 U.S.C. 103(a) as being unpatentable over Rossum et al. (U.S. 5,864,876) in view of what is old and well known in the art.

Regarding claim 26, Rossum et al. teach an electronic arithmetic-logic unit, comprising:

A main memory (Figure 1, item 18), the main memory including:

A first memory area subdivided into pages (Figure 3, item 18);

A second memory area (interpreted as a page table; column 1, lines 53 – 55 and column 5, line 17 both describe a page table in the memory), the first memory area being intended for data (interpreted as wavetable data; column 2, lines 2 – 4), and physical addresses of the pages of the first memory area being stored in the second memory area (Examiner notes that the page table contains the mapping to the physical addresses, as evidenced by column 3, lines 10 – 13).

Rossum et al. fail to explicitly teach a motherboard of an electronic arithmetic-logic unit. Examiner takes official notice that it is old and well known in this art for computer systems to include a CPU (Figure 1, item 10), memory (Figure 1, item 18), and multiple busses (Figure 1, items 22, 40, 12, 16) on a motherboard.

* * *

Claim 29 is rejected under 35 U.S.C. 103(a) as being unpatentable over Rossum et al. (U.S. 5,864,876) in view of Porterfield (U.S. 6,301,645) and Ritchie (U.S. 4,135,240).

Regarding claim 29, Rossum et al. teach an arithmetic-logic unit (Figure 1, item 10), the arithmetic-logic unit including a memory device (Figure 1, item 18) having a first memory area divided into pages (Figure 3, item 18) and a second memory area (interpreted as a page table; column 1, lines 53 – 55 and column 5, line 17 both describe a page table in the memory) storing physical addresses of the pages of the first memory area (Examiner notes that the page table contains the mapping to the physical addresses, as evidenced by column 3, lines 10 – 13), and an electronic unit (Figure 1, item 42), the electronic arithmetic-logic unit performing the following:

Transferring data between the memory device and the electronic unit (column 2, lines 46 – 50).

Rossum et al. fail to teach during the data transfer, autonomously transferring physical addresses from the second memory area to the electronic unit.

Porterfield teaches autonomously transferring physical addresses from the second memory area (interpreted as a remapping table; column 3, lines 23 – 32) to the electronic unit (interpreted as a source device and an address translator; Figure 4, item 405 describes transferring the physical addresses from the second memory area to the electronic unit during a data transfer. The motivation for this method, using the system controller of Porterfield, is to allow device requests to memory to be more efficient and maintain compatibility between different bus standards (column 1, lines 45 – 58). For

this reason, Examiner finds that the device of Porterfield is applicable to the multi-device, multi-bus system of Rossum et al. (as shown in Figure 1).

Therefore, it would have been obvious to one of ordinary skill in this art at the time of invention by Applicant to incorporate the system controller of Porterfield into the system of Rossum et al. for the purpose of making data transfers between devices and memory more efficient, while maintaining compatibility between different devices and different bus standards. This would have been obvious to improve the performance of the system of Rossum et al.

Rossum et al. and Porterfield fail to teach a computer program implementation of the above.

Ritchie teaches that computer hardware and software are functionally equivalent, and may preferably be substituted for one another in practice (column 5, lines 48 – 60).

Therefore, it would have been obvious to one of ordinary skill in this art at the time of invention by Applicant to implement the hardware means of Rossum et al. and Porterfield in software for the purpose of modifying the design more easily, and to facilitate debugging.

* * *

Claim 30 is rejected under 35 U.S.C. 103(a) as being unpatentable over Rossum et al. (U.S. 5,864,876) in view of Porterfield (U.S. 6,301,645) and Ritchie (U.S. 4,135,240).

Regarding claim 30, Rossum et al. teach an arithmetic-logic unit (Figure 1, item 10), the arithmetic-logic unit including a memory device (Figure 1, item 18) and an electronic unit (Figure 1, item 42) coupled via a data bus (Figure 1, items 22, 16), the memory device having a first memory area divided into pages (Figure 3, item 18) and a second memory area (interpreted as a page table; column 1, lines 53 – 55 and column 5, line 17 both describe a page table in the memory) storing physical addresses of the pages of the first memory area (Examiner notes that the page table contains the mapping to the physical addresses, as evidenced by column 3, lines 10 – 13), and an electronic unit (Figure 1, item 42), the electronic arithmetic-logic unit performing the following:

Transferring data between the memory device and the electronic unit (column 2, lines 46 – 50).

Rossum et al. fail to teach during the data transfer, autonomously transferring physical addresses from the second memory area to the electronic unit.

Porterfield teaches autonomously transferring physical addresses from the second memory area (interpreted as a remapping table; column 3, lines 23 – 32) to the electronic unit (interpreted as a source device and an address translator; Figure 4, item 405 describes transferring the physical addresses from the second memory area to the electronic unit during a data transfer. The motivation for this method, using the system controller of Porterfield, is to allow device requests to memory to be more efficient and maintain compatibility between different bus standards (column 1, lines 45 – 58). For

this reason, Examiner finds that the device of Porterfield is applicable to the multi-device, multi-bus system of Rossum et al. (as shown in Figure 1).

Therefore, it would have been obvious to one of ordinary skill in this art at the time of invention by Applicant to incorporate the system controller of Porterfield into the system of Rossum et al. for the purpose of making data transfers between devices and memory more efficient, while maintaining compatibility between different devices and different bus standards. This would have been obvious to improve the performance of the system of Rossum et al.

Rossum et al. and Porterfield fail to teach a memory device storing program code for implementation of the above.

Ritchie teaches that computer hardware and software are functionally equivalent, and may preferably be substituted for one another in practice (column 5, lines 48 – 60).

Therefore, it would have been obvious to one of ordinary skill in this art at the time of invention by Applicant to implement the hardware means of Rossum et al. and Porterfield in software for the purpose of modifying the design more easily, and to facilitate debugging.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Matthew D. Spittle whose telephone number is (571) 272-2467. The examiner can normally be reached on Monday - Friday, 8 - 4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark Rinehart can be reached on 571-272-3632. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

MDS

MARK H. RINEHART
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100